Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application.

Claims 1-4. Cancelled

5. (Original) An interface circuit for producing an output signal from an input signal and a reference signal, wherein the output signal has an output direct current (dc) voltage level that is substantially equal to a dc voltage level of the reference signal, the interface circuit comprising:

a level translation module adapted to generate an input level control signal from the reference signal;

a level adjustment module adapted to produce an adjusted buffer input signal from the input signal, wherein the adjusted buffer input signal has a dc voltage level that is substantially equal to a dc voltage level of the input level control signal; and

a buffer adapted to generate the output signal from the adjusted buffer input signal.

6. (Original) The interface circuit of claim 5, wherein said level translation module comprises:

a replica buffer adapted to generate a replica buffer output signal from the input level control signal; and

a difference amplifier having a positive input terminal adapted to receive the reference signal, a negative input terminal adapted to receive the replica buffer output signal, and an output terminal adapted to generate the input level control signal.

7. (Original) The interface circuit of claim 6, wherein the difference amplifier is an operational amplifier (op-amp).

8. (Original) The interface circuit of claim 6, wherein the buffer and the replica buffer both operate with substantially equal offsets.

9. (Original) The interface circuit of claim 5, wherein the output signal and the input signal are each single-ended signals.

10. (Original) The interface circuit of claim 9, wherein the buffer comprises:

a source-follower transistor adapted to generate the output signal from the adjusted buffer input signal;

a replica transistor adapted to generate a replica signal from the adjusted buffer input signal; and

a level shifting circuit that provides a level-shifted replica signal at a terminal of the source-follower transistor.

11. (Original) The interface circuit of claim 5, wherein the output signal and the input signal are each differential signals.

12. (Original) The interface circuit of claim 11, wherein the buffer comprises:

a source-follower transistor adapted to generate the output signal from the adjusted buffer input signal;

a replica transistor adapted to generate a replica signal from the adjusted buffer input signal; and

a level shifting circuit that provides a level-shifted replica signal at a terminal of the source-follower transistor.

13. (Original) The interface circuit of claim 5, wherein the buffer comprises a damping circuit.

14. (Original) The circuit of claim 13, wherein the damping circuit comprises a low pass filter.

15. (Original) A circuit, comprising:

a buffer;

a sampling circuit having a switch; and

a damping circuit coupled between the buffer and the sampling circuit;

wherein the damping circuit is adapted to reduce charge glitches when the switch closes.

16. (Original) The circuit of claim 15, wherein the damping circuit comprises a low pass filter.

17. (Original) The circuit of claim 16, wherein the low pass filter is an RC low pass filter.

18. (Original) The circuit of claim 15, wherein the buffer comprises:

a source-follower transistor adapted to generate an output signal from an input signal;

a replica transistor adapted to generate a replica signal from the input signal; and

a level shifting circuit that provides a level-shifted replica signal at a terminal of the source-follower transistor.